POSTAL BOOK PACKAGE 2027

ELECTRONICS ENGINEERING

CONVENTIONAL PRACTICE SETS VOLUME-IV

CONTENTS

BASIC ELECTRICAL ENGINEERING

CONVENTIONAL PRACTICE SETS

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1 CHAPTER
DC Machines

Q.1 An 8-pole dc generator has 500 armature conductors and a useful flux of 0.05 Wb. What will be the emf generated, if it is lap-connected and runs at 1,200 rpm? What must be the speed at which it is to be driven to produce the same emf, if it is wave-wound?

Solution:

EMF generated when the generator is lap-connected,

$$E_g = \frac{\phi ZN}{60} \times \frac{P}{A} = \frac{0.05 \times 500 \times 1{,}200}{60} \times \frac{8}{8} = 500 \text{ V}$$

$\because$ in lap-connected armature, number of parallel paths, $A = P = 8$

If the armature is wave connected, then

$\because$ in wave-connected armature $A = 2$

$$N' = \frac{E_g \times 60}{\phi \times Z} \times \frac{A}{P} = \frac{500 \times 60}{0.05 \times 500} \times \frac{2}{8} = 300 \text{ rpm}$$

Q.2 A 4-pole, 900 r.p.m. d.c. machine has a terminal voltage of 220 V and an induced voltage of 240 V at rated speed. The armature circuit resistance is 0.2 Ω. Is the machine operating as a generator or a motor? Compute the armature current and the number of armature coils if the air-gap flux/pole is 10 m Wb and the armature turns per coil are 8. The armature is wave-wound.

Solution:

Since the induced voltage E is more than the terminal voltage v, the machine is working as a generator.

$$E - V = I_a R_a \Rightarrow 20 = I_a \times 0.2 \Rightarrow I_a = 100 \text{ A}$$

Now, $$E_b = \frac{\phi ZN}{60} \times \left(\frac{P}{A}\right) \text{ or } 240 = 10 \times 10^{-3} \times Z \times \frac{900}{60} \times \frac{4}{2} \quad \Rightarrow Z = 800$$

Since there are 8 turns in a coil, it means there are 16 active conductors/coil. Hence, the number of coils $= \frac{800}{16} = 50$.

Q.3 A DC machine has total armature ampere conductors of 4500 and total flux in the machine is 0.14 Wb. Calculate the torque developed in the machine.

Solution:

The torque equation of a DC machine is $\tau = \frac{PZ}{2\pi A} \phi I_a$

where, P = Number of poles, Z = Total armature conductors, ϕ = Flux, I_a = Armature current and A = Number of parallel paths.

Let us assume lap winding

$\Rightarrow$ $A = P$

$\therefore$ $$\tau = \frac{Z I_a \phi}{2\pi}$$

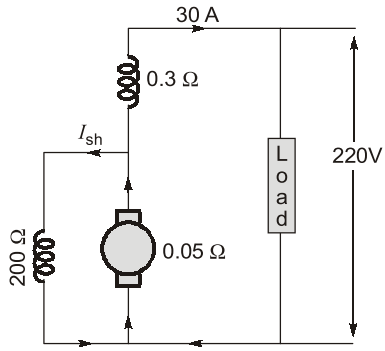
Given, $Z I_a = 4500$; $\phi = 0.14$ Wb

$$\tau = \frac{4500}{2\pi} \times 0.14 = 100.2676 \text{ Nm}$$

Q.4 A short-shunt compound generator delivers a load current of 30 A at 220 V, and has armature, series-field and shunt-field resistances of 0.05 Ω, 0.30 Ω and 200 Ω respectively. Calculate the induced e.m.f. and the armature current. Allow 1.0 V per brush for contact drop.

Solution:

Short-shunt compound Generator circuit diagram is shown in figure.



Voltage drop in series winding = $30 \times 0.3 = 9$ V

Voltage across shunt winding = $220 + 9 = 229$ V

$$I_{sh} = \frac{229}{200} = 1.145\,\text{A}$$

$I_a = 30 + 1.145 = 31.145$ A

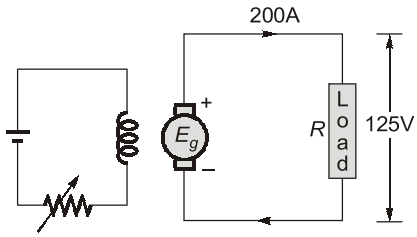
$I_a R_a = 31.145 \times 0.05 = 1.56$ V

Brush drop = $2 \times 1 = 2$ V

$E_g = V$ + Brush drop + $I_a R_a$ + Series drop = $220 + 9 + 2 + 1.56 = 232.56$ V

Q.5 A separately excited generator, when running at 1000 r.p.m. supplied 200 A at 125 V. What will be the load current when the speed drops to 800 r.p.m. if I_f is unchanged? Given brush drop = 2 V and armature resistance = 0.04 Ω.

Solution:



Given data: The load resistance, $R = \frac{125}{200} = 0.625\ \Omega$, in figure.

$E_{g1} = 125 + 200 \times 0.04 + 2 = 135$ V

$N_1 = 1000$ r.p.m.

Since, $E_g \propto N$. Therefore, $E_{g2} = E_{g1} \cdot \frac{N_2}{N_1}$

At 800 r.p.m. $E_{g2} = 135 \times \frac{800}{1000} = 108$ V

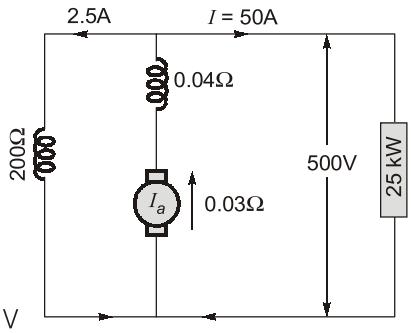
if I is the new load current, then terminal voltage V is given by

$$V = 108 - 0.04\,I - 2 = 106 - 0.04\,I$$

$$I = \frac{V}{R} = \frac{(106 - 0.04I)}{0.625} = 159.4\ \text{A}$$

Q.6 A 4-pole, long-shunt lap-wound generator supplies 25 kW at a terminal voltage of 500 V. The armature resistance is 0.03 ohm, series field resistance is 0.04 ohm and shunt field resistance is 200 ohm. The voltage drop per brush may be taken as 1.0 V. Determine the e.m.f. generated.
Calculate also the No. of conductors if the speed is 1200 r.p.m. and flux per pole is 0.02 weber. Neglect armature reaction.

Solution:



$$I = \frac{25000}{500} = 50\ \text{A}$$

$$I_{sh} = \frac{500}{200} = 2.5\ \text{A}$$

$I_a = I + I_{sh} = 50 + 2.5 = 52.5$ A

Series field drop = $52.5 \times 0.04 = 2.1$ V

Armature drop = $52.5 \times 0.03 = 1.575$ V

Brush drop = $2 \times 1 = 2$ V

Generated e.m.f., $E_g = 500 + 2.1 + 1.575 + 2 = 505.68$ V

Generated emf, $E_g = \frac{\phi ZN}{60} \times \left(\frac{P}{A}\right)$ $A = P$ ($\because$ Lap-wound)

$\therefore$ $Z = \frac{60E_g}{N\phi} = \frac{60 \times 505.68}{1200 \times 0.02} = 1264.2$

Number of conductors, $Z \simeq 1264$

Q.7 The following information is given for a 300 kW, 600-V, long-shunt compound generator: Shunt field resistance = 75 Ω, armature resistance including brush resistance = 0.03 Ω, commutating field winding resistance = 0.011 Ω, series field resistance = 0.012 Ω, diverter resistance = 0.036 Ω. When the machine is delivering full load, calculate the voltage and power generated by the armature.

Solution:

Given data: Power output = 300,000 W; Output current = $\frac{300000}{600}$ = 500 A

$I_{sh} = \frac{600}{75}$ = 8 A; I_a = 500 + 8 = 508 A

A diverter is a resistance shunting the series field resistance of compound generator to adjust the degree of compounding to produce a desired voltage regulation.

Since the series field resistance and diverter resistance are in parallel their combined resistance is

$= \frac{0.012 \times 0.036}{0.048} = 0.009\,\Omega$

Total armature circuit resistance = 0.03 + 0.011 + 0.009

= 0.05 Ω

Voltage drop = 508 × 0.05

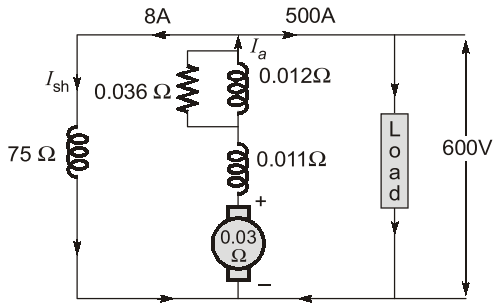
= 25.4 V

Voltage generated by armature = 600 + 25.4 = 625.4 V

Power generated = 625.4 × 508

= 317,700

Power generated in kW = 317.7 kW



Q.8 A shunt generator has a full load current of 196 A at 220 V. The stray losses are 720 W and the shunt field coil resistance is 55 Ω. If it has a full load efficiency of 88%, find the armature resistance. Also, find the load current corresponding to maximum efficiency.

Solution:

Output = 220 × 196 = 43,120 W; η = 88% (overall efficiency)

Electrical input = $\frac{43120}{0.88}$ = 49,000 W

Total losses = 49,000 – 43,120 = 5,880 W

Shunt field current = $\frac{220}{55}$ = 4 A $\therefore$ I_a = 196 + 4 = 200 A

$\therefore$ Shunt Cu loss = 220 × 4 = 880 W ; Stray losses = 720 W

Constant losses = 880 + 720 = 1,600 W

$\therefore$ Armature Cu loss = 5,880 – 1,600 = 4,280 W

$\therefore$ $I_a^2 R_a$ = 4,280 W

$200^2 R_a$ = 4,280 or R_a = 4,280/200 × 200 = 0.107 Ω

For maximum efficiency $I^2 R_a$ = constant losses = 1,600 W; $I = \sqrt{\frac{1600}{0.107}} = 122.28$ A

Q.9 A long-shunt compound-wound generator gives 240 volts at full load output of 100 A. The resistances of various windings of the machine are: armature (including brush contact) 0.1 Ω, series field 0.02 Ω, interpole field 0.025 Ω, field (including regulating resistance) 100 Ω. The iron loss at full load is 1000 W; windage and friction losses total 500 W. Calculate full load efficiency of the machine.

Solution:

Output = $240 \times 100 = 24{,}000$ W

Total armature circuit resistance = $0.1 + 0.02 + 0.025 = 0.145\ \Omega$

$$I_{sh} = \frac{240}{100} = 2.4 \text{ A}$$

$$\therefore \quad I_a = 100 + 2.4 = 102.4 \text{ A}$$

$\therefore$ Armature circuit copper loss = $(102.4)^2 \times 0.145 = 1{,}521$ W

Shunt field copper loss = $2.4 \times 240 = 576$ W

Iron loss = 1000 W; Friction loss = 500 W

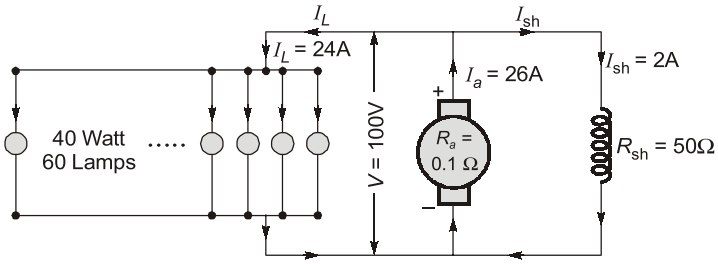
Total loss = $1{,}521 + 1{,}500 + 576 = 3{,}597$ W; $\eta = \dfrac{24{,}000}{24{,}000 + 3{,}597} \times 100 = 87\%$

Q.10 A 4-pole generator with lap-connected armature having field and armature resistances of 50 Ω and 0.1 Ω respectively supplies 60, 40 W lamps at 100 V. Calculate the total armature current, current per path and the generated emf. Assume a constant drop of 1 V per brush.

Solution:

Total lamp load, P_L = Number of lamps × wattage of each lamp = $60 \times 40 = 2{,}400$ W

Terminal voltage, $V = 100$ V



Load current, $I_L = \dfrac{P_L}{V} = \dfrac{2{,}400}{100} = 24$ A

Shunt field current, $I_{sh} = \dfrac{V}{R_{sh}} = \dfrac{100}{50} = 2$ A

Total armature current, $I_a = I_L + I_{sh} = 24 + 2 = 26$ A

$\because$ For lap-connected $A = P = 4$

Current per path, $I_c = \dfrac{I_a}{A} = \dfrac{26}{4} = 6.5$ A

Generated emf, $E_g = V + I_a R_a$ + brush drop $= 100 + (26 \times 0.1) + (2 \times 1) = 104.6$ V

Q.11 A 250 V dc shunt motor having an armature resistance of 0.25 Ω carries an armature current of 50 A and runs at 750 rpm. If the flux is reduced by 10%, find the speed. Assume that the torque remains the same.

Solution:

Supplied Voltage, $V = 250$ V

Armature current, $I_{a1} = 50$ A

Back emf, $E_{b1} = V - I_{a1} R_a = 250 - 50 \times 0.25 = 237.5$ V

Flux, $\phi_2 = 0.9\,\phi_1$

$\because$ Flux has been reduced by 10%

Since torque developed remains unchanged,

$$I_{a2}\phi_2 = I_{a1}\phi_1 \text{ as } T \propto \phi I_a$$

or Armature current, $$I_{a2} = I_{a1} \times \frac{\phi_1}{\phi_2} = 50 \times \frac{1}{0.9} = 55.55 \text{ A}$$

Back emf, $$E_2 = V - I_{a2} R_a = 250 - 55.55 \times 0.25 = 236.11 \text{ V}$$

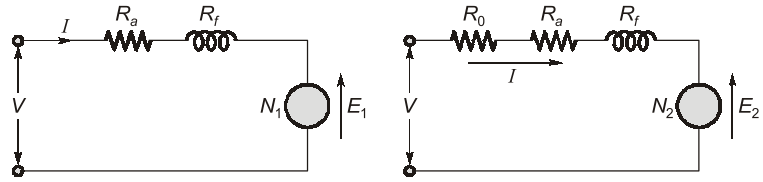
$\because$ $$E_b \propto \phi N$$

Speed, $$N_2 = \frac{E_{b2}}{E_{b1}} \times \frac{\phi_1}{\phi_2} \times N_1 = \frac{236.11}{237.5} \times \frac{1}{0.9} \times 750 = 828.5 \text{ rpm}$$

Q.12 A series motor has an armature resistance of 0.7 ohm and field resistance of 0.3 ohm. It takes a current of 15 A from a 200 V supply and runs at 800 r.p.m. Find the speed at which it will run, when connected in series with a 5 ohm resistance and taking the same current at the same supply voltage.

Solution:

Given data: $R_a = 0.7\ \Omega$; $R_f = 0.3\ \Omega$; $R_0 = 5\ \Omega$; $I = 15$ A; $V = 200$ V; $N_1 = 800$ rpm



We have to calculate N_2.

We know that, $$E \propto \phi N$$ [ϕ = Field flux]

But, as I has not changed, so ϕ will remain same in this case,

$\Rightarrow$ $$E \propto N$$

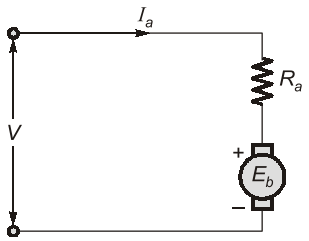
$\Rightarrow$ $$\frac{E_1}{E_2} = \frac{N_1}{N_2} \quad \ldots(1)$$

Now, $$E_1 = V - I(R_a + R_f)$$
$$= 200 - 15(1) = 185 \text{ V}$$
$$E_2 = V - I(R_a + R_f + R_0)$$
$$= 200 - 15(6) = 110 \text{ V}$$

From equation (1), $$N_2 = \frac{N_1 E_2}{E_1} = \frac{800 \times 110}{185} = 475.6756 \text{ rpm}$$

Q.13 A DC motor with permanent magnet field is running with 200 V DC supply and consuming 2 A current. A voltmeter is connected across its armature and DC supply is disconnected. The voltmeter reads 190 V just after disconnection of DC supply. Calculate the armature resistance of the machine.

Solution:



Equivalent circuit of the motor

Given data: $V = 200$ V; $I_a = 2$ A; $E_b = 190$ V this is present because of field magnets

We can write, $$V = I_a R_a + E_b$$ [Neglecting voltage drop across brushes]

$\Rightarrow$ $$200 = 2R_a + 190$$

$\Rightarrow$ $$R_a = 5\ \Omega$$

ADVANCED COMMUNICATION

CONVENTIONAL PRACTICE SETS

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1 CHAPTER

Microwave Communication

Q.1 What is "skip distance"? Why there is better high frequency reception during night time?
A long distance microwave link consists of a chain of repeaters at 40 km intervals. What must be the minimum height of transmitting and receiving antennas above ground level? (The antennas are identical to each other in order to ensure line of sight communication).

Solution:

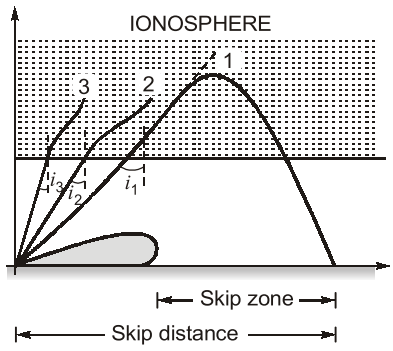
Skip distance can be defined as:

1. The minimum distance from the transmitter at which a sky wave of given frequency is returned to earth by ionospheric layer.
2. The minimum distance from the transmitter to a point where sky wave of a given frequency is received.
3. The minimum distance within which a sky wave of given frequency fails to reflect back.

There is a zone which is not covered by any wave (surface or sky wave) called skip zone.

During night time layer F_1 and F_2 combines and form one layer called F layer and D-region vanishes altogether. Thus in night time only two principal layer exits i.e. E & F layer.

So there is better high frequency reception during night time.



Distance between repeaters $d = 40$ km,
when there is no atmosphere.

$$d(\text{km}) = 3.57\left[\sqrt{h_t} + \sqrt{h_r}\right]$$

$$40 = 3.57[2\sqrt{h}] \qquad \text{given } [h_t = h_r]$$

where, h_t = height of transmitter in antenna in meters and h_r = height of receiving antenna in meter

$$h_t = h_r = 31.38 \text{ m}$$

When atmosphere is present, $d = 4.12\left[\sqrt{h_t} + \sqrt{h_r}\right]$

$$40 = 4.12[2\sqrt{h}]$$

$$h_t = h_r = 23.56 \text{ m}$$

Q.2 The critical frequencies at an instant observed for E, F_1 and F_2 layers were found to be 3, 5 and 9 MHz. Find the corresponding concentration of electrons in these layers.

Solution:

Given: Critical frequencies for E layer = 3 MHz, critical frequencies for F_1 layer = 5 MHz, critical frequencies for F_2 layer = 9 MHz.

To be calculated: Concentration of electrons.

$$f_c = 9\sqrt{N_{max}} \qquad \Rightarrow N_{max} = \frac{f_c^2}{81}$$

For E layer, $f_c = 3$ MHz $\qquad \Rightarrow N_{max} = \dfrac{f_c^2}{81} = 9 \times \dfrac{10^{12}}{81} = 0.111 \times 10^{12}$ Electrons/m^3

For F_1 layer, $f_c = 5$ MHz $\Rightarrow N_{max} = \frac{f_c^2}{81} = 25 \times \frac{10^{12}}{81} = 0.3086 \times 10^{12}$ Electrons/m^3

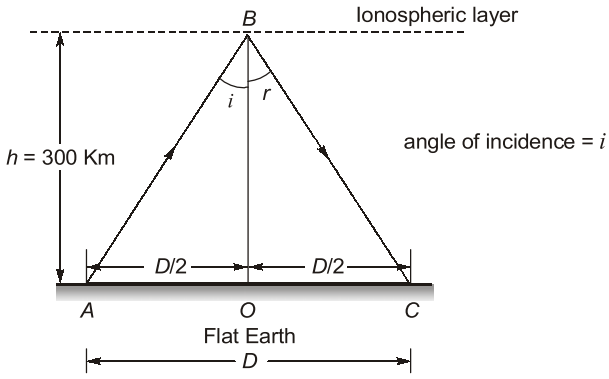
For F_2 layer, $f_c = 9$ MHz $\Rightarrow N_{max} = \frac{f_c^2}{81} = 81 \times \frac{10^{12}}{81} = 10^{12}$ Electrons/m^3

Q3 For an ionospheric layer at a height of 300 km, having electron concentration of 5×10^{11} per m^3. Find the maximum permissible frequency at an angle of incidence of 60°. Calculate the critical frequency and skip distances, under flat earth assumptions.

Solution:

Under Flat Earth assumptions we have,

From ΔAOB,



$$\cos i = \frac{BO}{AB} = \frac{h}{\sqrt{h^2 + D^2/4}}$$

$$= \frac{2h}{\sqrt{4h^2 + D^2}}$$

$$\Rightarrow \cos 60° = \frac{2 \times 300}{\sqrt{4 \times (300)^2 + D^2}}$$

$$\Rightarrow 4 \times (300)^2 + D^2 = (1200)^2$$

$$\Rightarrow D^2 = 1080{,}000$$

$\Rightarrow$ D = Propagation distance AC = 1039.23 km = Skip – distance

Also, ionization density (electrons per cubic meter) = $N_{max} = 5 \times 10^{11}$ / m^3

$\therefore$ f_c = Critical frequency for the layer

$= 9\sqrt{N_{max}} = 9\sqrt{5 \times 10^{11}} = 6{,}36{,}3961.03$ Hz $= 6.36 \times 10^6$ Hz $= 6.36$ MHz

Now, maximum permissible frequency under flat earth assumptions is,

$$f_{muf} = f_c\sqrt{1 + \left(\frac{D}{2h}\right)^2} = 6.36 \times 10^6\sqrt{1 + \left(\frac{1039.23}{600}\right)^2} = 12.719 \times 10^6 \text{ Hz}$$

$$\approx 12.72 \text{ MHz}$$

Q4 A high frequency radio link has to be established between two points at a distance of 2500 km on the earth's surface. Considering ionospheric height to be 200 km and its critical frequency 5 MHz, calculate the maximum usable frequency for the given path.

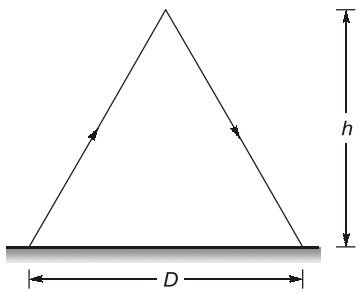
Solution:

Given: $D = 2500$ km, $h = 200$ km and $f_c = 5$ MHz

Maximum Usable frequency is,

$$f_{muf} = f_c\sqrt{1 + \left(\frac{D}{2h}\right)^2}$$

$$\Rightarrow f_{muf} = 5\sqrt{1 + \left(\frac{2500}{2 \times 200}\right)^2} = 31.65 \text{ MHz}$$



Q.5 Calculate the skip distance for flat earth with MUF of 10 MHz if the wave is reflected from a height of 300 km where the maximum value of refractive index (n) is 0.9.

Solution:

Given: MUF = 10 MHz, height (h) = 300 km and $n = 0.9$.

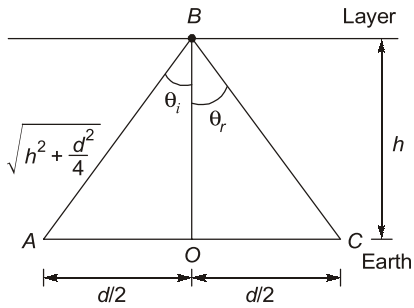
To be calculated: Skip distance.

$$n^2 = 0.81 = (1 - 81N/f^2)$$
$$N_{max} = (1 - n^2) f^2/81 = [(1 - 0.81) \times 10^{14}]/81 = (19/81) \times 10^{12}$$
$$= 23.45 \times 10^{10} \text{ Electrons/m}^3$$
$$f_c = 9\sqrt{N_{max}} = 9\sqrt{(23.45 \times 10^{10})} = 9 \times 4.8425 \times 10^5 = 4.36 \text{ MHz}$$
$$d_{skip} = 2h\sqrt{[(f_{MUF}/f_c)^2 - 1]} = 2 \times 300\sqrt{\left[(10/4.36)^2 - 1\right]} = 600 \times 2.06$$
$$= 1236 \text{ km}$$

Q.6 Calculate the maximum single hop distance for D, E, F_1 and F_2 layers if their heights are assumed to be 70, 130, 230 and 350 km respectively above the earth and the angle of incidence is 10° in all cases.

Solution :

To be calculated: Skip distance (d)



$$\cos\theta_i = \frac{OB}{AB}$$
$$\cos\theta_i = \frac{h}{\sqrt{h^2 + d^2/4}} = \frac{2h}{\sqrt{4h^2 + d^2}}$$
$$\cos^2\theta_i = \frac{4h^2}{4h^2 + d^2}$$
$$4h^2(\cos^2\theta_i - 1) = -d^2\cos^2\theta_i$$
$$d^2\cos^2\theta_i = 4h^2(1 - \cos^2\theta)$$
$$d^2 = 4h^2(\sec^2\theta_i - 1)$$
$$\boxed{d = 2h\sqrt{(\sec^2\theta_i - 1}}$$
$$d = 2h\sqrt{(\sec 10)^2 - 1} = 2h \times 0.176 = 0.352h$$

For D layer, $d = 0.352h = 0.352 \times 70 = 24.64$ km
For E layer, $d = 0.352h = 0.352 \times 130 = 45.76$ km
For F_1 layer, $d = 0.352h = 0.352 \times 230 = 80.96$ km
For F_2 layer, $d = 0.352h = 0.352 \times 350 = 123.2$ km

Q.7 In a microwave communication link operating at 100 MHz, the respective heights of transmitting and receiving antennas are 49 m and 25 m respectively. If the transmitted power is 100 W, then determine:

(i) The line of sight (LOS) distance.

(ii) The electric field strength received at LOS distance.

Solution:

Operating frequency, $f = 100$ MHz
Transmitted power, $P_t = 100$ W
Height of transmitting antenna, $h_t = 49$ m
Height of receiving antenna, $h_r = 25$ m

(i) Calculating the LOS distance:

$$\text{LOS distance} = 4.12\left(\sqrt{h_t} + \sqrt{h_r}\right) \text{ km}$$

Here, h_t and h_r must be represented in meters to get the value of LOS distance in kilometers.

So, $$\text{LOS distance} = 4.12\left(\sqrt{49} + \sqrt{25}\right) \text{ km} = 49.44 \text{ km}$$

(ii) Calculating the electric field strength received at LOS distance:

Electric field strength received (E_r) at a distance "d" from the transmitter can be given by,

$$E_r = \frac{88\sqrt{P_t}}{\lambda d^2} h_t h_r$$

Here, $$\lambda = \text{wavelength} = \frac{c}{f} = \frac{3\times10^8}{100\times10^6}\text{ m} = 3\text{ m}$$

$$d = \text{LOS distance} = 49.44 \text{ km}$$

So, $$E_r = \frac{88\sqrt{100}}{(3)(49.44\times10^3)^2}(49\times25)\text{ V/m} = 147\ \mu\text{V/m}$$

Q.8 Distinguish between radio horizon and optical horizon.

Solution:

Radio Horizon	Optical Horizon
1. Microwaves do not bend or refract beyond the radio horizon.	1. Microwaves are usually bent or refracted beyond the optical horizon
2. This horizon is not visible to our eyes, because generally these are further away from the optical horizon.	2. This horizon is visible to our eyes.
3. The distance to radio horizon varies with the atmospheric refractive changes.	3. The optical horizon is independent of atmospheric refractive changes.
4. The distance to the radio horizon is given by $d_r = 0.49\text{ h km}$ where h = height of tower	4. The distance to the optical horizon is given by $d_r = 0.49\sqrt{h}$ km where h = Height of tower
5. Radio horizon distance can also be calculated as $d_r = \frac{d_o}{K}$ where K = Correction factor	5. Optical horizon distance can also be calculated as $d_o = Kd_r$ where K = Correction factor
6. If $K < 1$, the radio horizon is further away from optical horizon.	6. If $K > 1$, optical horizon is further away from radio horizon.

Q.9 A TV transmitting antenna has a height of 169 meters and receiving antenna has a height of 16 m. What is the maximum distance through which the TV signal could be received by space wave propagation? Also calculate the Radio horizon in this case.

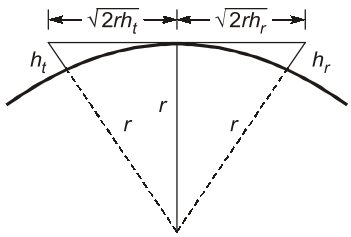
Solution:

Given that, $H_T = 169$ m, $H_R = 16$ m

$\therefore$ Maximum distance of LOS (d) $= 4.12\left(\sqrt{h_t} + \sqrt{h_r}\right)$km

$\Rightarrow$ $$d = 4.12\left(\sqrt{169} + \sqrt{16}\right) = 4.12\times17$$

$\therefore$ $$d = 70.04 \text{ km}$$



we know that the radio horizon is the distance at which direct rays from a radio transmitter become tangential to the earth's surface.

ADVANCED ELECTRONICS

CONVENTIONAL PRACTICE SETS

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1 CHAPTER
Introduction to VLSI Technology

Q.1 Compare the merits and demerits of CMOS integrated circuits vis-a-vis those of bipolar integrated circuit.

Solution:

	CMOS integrated circuit		Bipolar integrated circuit
1.	Power consumption is very low.	1.	Power consumption is relatively high.
2.	Packing density is very high.	2.	Packing density is comparatively low.
3.	Speed of operation is low compare to bipolar integrated circuit	3.	Speed of operation is relatively high.
4.	Noise margin is very high.	4.	Noise margin is high in one case in other case it is lower than that of CMOS integrated circuit.
5.	Fan out is very high.	5.	Fan out is relatively low.
6.	Frequency of operation is comparatively lower than that of bipolar integrated circuits.	6.	Frequency of operation can be high.
7.	Offers high input impedance, is excellent for constructing simple, low power logic gates.	7.	Input impedance is low therefore power consumption is relatively higher.

Q.2 Why do we use silicon in IC fabrication?

Solution:

- The fabrication of semiconductor devices has been based on the use of silicon as the premier semiconductor. Two other semiconductors, germanium (Ge) and gallium arsenide (GaAs), present special problems while silicon has certain specific advantages not available with the others.
- At 300°K silicon has a band gap of 1.12 eV, while germanium's band gap is 0.66 eV. Because of this small band gap, the intrinsic carrier density of germanium at $T = 300°K$ is about $2.5 \times 10^{13} cm^{-3}$. At temperatures of about 400°K, this density becomes $10^{15} cm^{-3}$, which is comparable to the lower range of doping densities used. This property limits its use to low temperature applications at less than 350°K.
- The other semiconductor of major interest is gallium arsenide. In spite of its attractive electrical properties, gallium arsenide crystals have a high density of crystal defects, which limits the performance of devices made from it.
- Silicon is an abundant element and occurs naturally in the form of sand. It can be refined using simple purification and crystal growth techniques. It also exhibits suitable physical properties for fabricating active devices with good electrical characteristics. In addition silicon can be easily oxidized to form an excellent insulator, (SiO_2) or glass.
- This native oxide is useful, for constructing capacitors and MOSFET's. It also serves as a diffusion barrier that masks against unwanted impurities from diffusing into the high purity silicon material. This masking property allows selective alternation of electrical properties in the silicon.

Q3 How is electronic grade silicon crystal is obtained?

Solution:

Silicon is the most important semiconductor material used in electronic industry. It is found abundantly in nature in the form of silica and silicate (sand). The main raw material for growth of single silicon crystal is Electronic Grade Silicon (EGS), which is a polycrystalline material of high purity. The major impurities in EGS are boron, carbon and residual donors. To produce EGS, first Metallurgical Grade Silicon (MGS) is produced in a submerged-electrode arc furnace, which is charged with quartzite and carbon. Quartzite is relatively a pure form of sand (SiO_2). The overall reaction for producing MGS is

$$SiC\ (solid) + SiO_2\ (solid) \rightarrow Si\ (liquid) + SiO\ (gas) + CO\ (gas)$$

The drawn MGS is solidified at a purity of 98%. The next step is to crush the silicon and then react it with anhydrous hydrogen chloride to form trichlorsilane ($SiHCl_3$). The reaction is

$$Si\ (solid) + 3HCl\ (gas) \rightarrow SiHCl_3\ (gas) + H_2\ (gas) + heat$$

The reaction takes place in a fluidized bed at a temperature of 300°C to produce trichlorsilane in the presence of catalyst. Trichlorsilane is liquid at room temperature and it has many unwanted chlorides which can be removed by fractional distillation.

The EGS is prepared from purified $SiHCl_3$ in a chemical vapour deposition (CVD) process. The chemical reaction for EGS production is

$$2SiHCl_3\ (gas) + 2H_2\ (gas) \rightarrow 2Si\ (solid) + 6HCl\ (gas)$$

This reaction is also called **hydrogen reduction process.** An alternative method for producing EGS is pyrolysis of silane, which has lower production cost and less harmful reaction by-products. In this process, CVD reactor is operated at 900°C and supplied with silane instead of trichlorsilane. The pyrolysis reaction is

$$SiH_4\ (gas) + Heat \rightarrow Si\ (solid) + 2H_2\ (gas)$$

The EGS is in pure form of silicon but in the polycrystalline form. This polycrystalline silicon cannot be used for wafer manufacture. The next step is to grow a single silicon crystal which is usually done via the Czochralski (pronounced "Cha-krawl-ski") method.

Q4 If a silicon dioxide (SiO_2) layer of thickness 100 nm is grown by thermal oxidation, what is the thickness of silicon (Si) being consumed? Derive the relation used. The molecular weight of Si is 28.1 g/mol, and the density of Si is 2.33 g/cm^3. The corresponding values for SiO_2 are 60.08 g/mol and 2.21 g/cm^3.

Solution:

The volume of 1 mol of silicon is,

$$\frac{\text{Molecular weight of Si}}{\text{Density of Si}} = \frac{28.1\,\text{g/mol}}{2.33\,\text{g/cm}^3} = 12.06\ \text{cm}^3/\text{mol}$$

The volume of 1 mol of silicon dioxide is,

$$\frac{\text{Molecular weight of } SiO_2}{\text{Density of } SiO_2} = \frac{60.08\,\text{g/mol}}{2.21\,\text{g/cm}^3} = 27.18\ \text{cm}^3/\text{mol}$$

Since 1 mol of silicon is converted to 1 mol of silicon dioxide,

$$\frac{\text{Thickness of Si} \times \text{area}}{\text{Thickness of } SiO_2 \times \text{area}} = \frac{\text{Volume of 1 mol of Si}}{\text{Volume of 1 mol of } SiO_2}$$

$$\frac{\text{Thickness of Si}}{\text{Thickness of } SiO_2} = \frac{12.06}{27.18} = 0.44$$

$$\text{Thickness of Si} = (0.44)\,(\text{Thickness of } SiO_2)$$

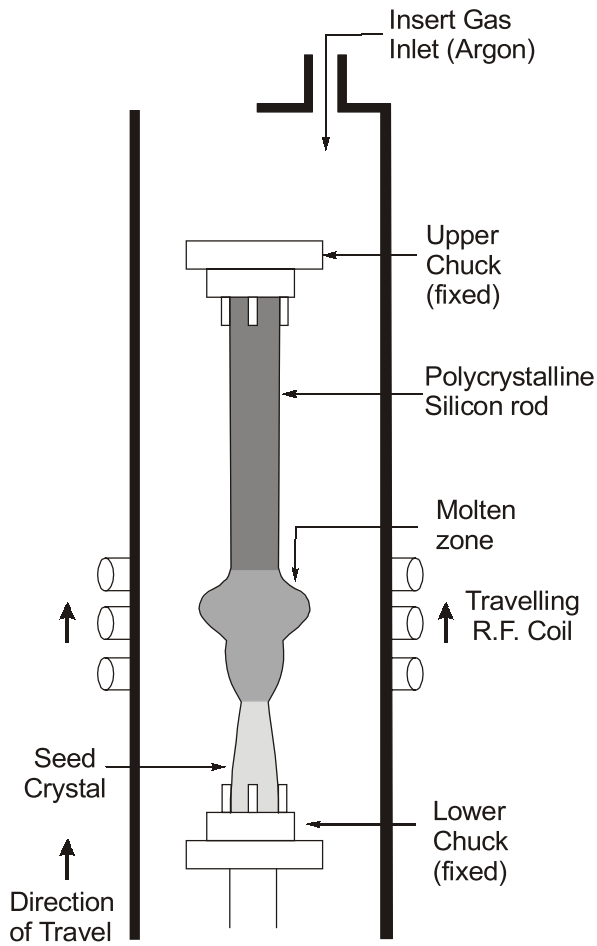
To grow a SiO_2 layer of 100 nm, the thickness of Si consumed will be,

$$\text{Thickness of Si} = (0.44)\,(100) = 44\ \text{nm}$$

Q.5 Explain briefly the float-zone crystal growth process with a neat diagram.

Solution:

The float-zone process can be used to grow silicon that has lower contaminations than that normally obtained from the Czochralski technique. A schematic setup of the float zone process is shown in the figure.



A high purity polycrystalline rod with a seed crystal at the bottom is held in a vertical position and rotated. The rod is enclosed in a quartz envelope within which an inert atmosphere (argon) is maintained.

During the operation, a small zone (a few centimeters in length) of the crystal is kept molten by a radio-frequency heater, which is moved from the seed upward so that this floating zone traverses the length of the rod. The molten silicon is retained by surface tension between the melting and growing solid-silicon faces. As the floating zone moves upward, a single-crystal silicon freezes at the zone's retreating end and grows as an extension of the seed crystal and the solidified region has the same orientation as the seed.

Materials with higher resistivities can be obtained from the float-zone process than from the Czochralski process because it can be used to purify the crystal more easily. The furnace is filled with an inert gas like argon to reduce gaseous impurities. Also, since no crucible is needed, it can be used to produce oxygen 'free' Si wafers.

At the present time, float-zone crystals are used mainly for high-power, high-voltage devices, where high-resistivity materials are required.

The difficulty is to extend this technique for large wafers, since the process produces large number of dislocations.

Q.6 Explain briefly the following process techniques involved in IC fabrication:

(i) Diffusion (ii) Ion implantation

Solution:

(i) **Diffusion:** Diffusion is the movement of impurity atoms in a semiconductor material at high temperatures. The driving force of diffusion is the concentration gradient. There is a wide range of diffusivities for various dopant species, which depend on how easy the respective dopant impurity can move through the material. Diffusion is applied to anneal the crystal defects after ion implantation or to introduce dopant atoms into silicon from a chemical vapour source. In the lateral case the diffusion time and temperature determine the depth of dopant penetration. But diffusion can also be an unwanted parasitic effect, because it takes place during all high temperature process steps.

The biggest limitation of thermal diffusion is that the process is isotropic, i.e. lateral diffusion cannot be avoided, though diffusion coefficients in different crystallographic directions might be different. Thus, an oxide window that serves as a mask to protect certain regions of the wafers can be ineffective due to lateral diffusion. This is especially important for doping small regions. Doping control is also difficult to achieve due to presence of concentration gradients. These gradients will change in subsequent annealing steps. Thus, there is a thermal budget associated with doping.

(ii) Ion implantation: Ion implantation is a relatively newer doping technique that operates close to room temperature. It is a physical process of doping, not based on a chemical reaction. It is the dominant technique to introduce dopant impurities into crystalline silicon. This is performed with an electric field which accelerates the ionized atoms or molecules so that these particles penetrate into the target material until they come to rest because of interactions with the silicon atoms.

Ion implantation is able to control exactly the distribution and dose of the dopants in silicon, because the penetration depth depends on the kinetic energy of the ions which is proportional to the electric field. The dopant dose can be controlled by varying the ion source. Since ion implantation takes place close to room temperature, it is compatible with conventional lithographic processes, so small regions can be doped. Also, since temperature is low, lateral diffusion is negligible.

Unfortunately, after ion implantation the crystal structure is damaged which implies worse electrical properties. Another problem is that the implanted dopants are electrically inactive, because they are situated on interstitial sites. Therefore after ion implantation a thermal process step is necessary which repairs the crystal damage and activates the dopants.

Q.7 A *p-n* junction is to be formed at a depth of 1 μm from the surface of an *n*-type Si substrate, which has a doping concentration of 10^{17} phosphorus atoms/cm^3. The junction is formed by a two-step diffusion of boron: the pre-deposition is solid-solubility limited at 1000°C and the drive-in is at 1100°C.

After the drive-in step, the surface concentration of boron is 5×10^{19} atoms/cm^3. Find out the appropriate diffusion times required for both the steps (pre-deposition and drive-in).

Assume the following data:

Diffusion constant for boron diffusion (D_0) = 10.5 cm^2/sec

The activation energy for boron diffusion (E_a) = 3.69 eV

The solid solubility limit of boron in silicon at 1000°C = 2×10^{20} atoms/cm^3

Solution:

Given data: Junction depth, $x_j = 1$ mm ; Doping concentration of substrate, $N_B = 10^{17}$/cm^3

Solid solubility limit of boron, $N_0 = 2 \times 10^{20}$/cm^3 ; Final surface concentration of boron, $N_S = 5 \times 10^{19}$/cm^3

Temperature used for pre-deposition, $T_1 = 1000 + 273$ K = 1273 K

Temperature used for drive-in, $T_2 = 1100 + 273$ K = 1373 K

Diffusion constant for boron, $D_0 = 10.5$ cm^2/sec

Activation energy for boron, $E_a = 3.69$ eV

Useful relations :

The concentration profile of the diffused atoms inside the substrate for pre-deposition process can be given as,

$$N(x, t) = N_0 \text{erfc}\left[\frac{x}{2\sqrt{Dt}}\right]$$

Where, erfc(t) = complementary error function, D = Diffusivity = $D_0 e^{-E_a/kT}$

t = process time used for diffusion and x = depth from the surface of the substrate

The concentration profile of the diffused atoms inside the substrate for drive-in process can be given as,

$$N(x, t) = \frac{Q_0}{\sqrt{\pi Dt}} e^{-x^2/4Dt} = N_S e^{-x^2/4Dt}$$

Where, Q_0 =Amount of solute per unit area present on the surface prior to drive-in

$$Q_0 = 2N_0\sqrt{\frac{D_1 t_1}{\pi}}$$

Here, D_1 = Diffusivity used in pre-deposition process and t_1 = process time of pre-deposition

After drive-in process, at junction depth (x_j), the concentration of solute (or diffused atoms) equals to the initial doping concentration of the substrate (or background concentration).

COMPUTER ORGANIZATION AND ARCHITECTURE

CONVENTIONAL PRACTICE SETS

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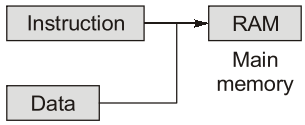
1 CHAPTER
Computer Organization

Q.1 Describe computer block diagram and list its internal components.

Solution:

Computer is a computational machine, used to process data under the control of a program. Computer system is implemented using Von Neumann architecture which says that instruction and data both are present in main memory.



Computer system contains 3-fundamental components:

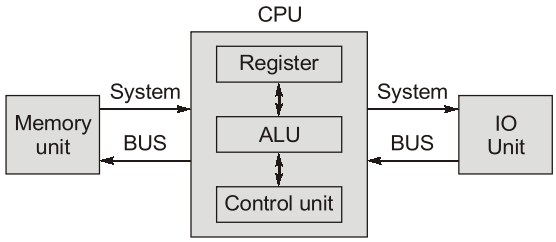
(i) **Central Processing Unit (CPU) :** . It contains 3 internal components
→ Registers → ALU → Control unit.

(ii) **Memory:** It is the storage component of computer. Memory chip is organised into cells called as addressable unit.

Ex: 64 KB RAM = 64 K × B → Cell Size
↓
Cells in chip

(iii) **IO:** It is external communication unit. It is of two kind as

(a) Input devices ($\overline{IORD}$) (b) Output devices ($\overline{IOWR}$)



Q.2 Explain different instruction format possible in computer design.

Solution:

CPU organisation is classified into 3-type:

(i) **Stack CPU :** In this organisation ALU operations are performed only on a stack data means both of the operands are always present in stack. After processing result is also present in stack.

(ii) **Accumulator CPU :** In this organisation ALU's 1st operand is always required in the accumulator and 2nd operand is present either is register or memory.
After processing result is always present in accumulator.

(iii) Register CPU :

(a) Register to memory reference CPU: In this organisation ALU 1st operand is always required in register and 2nd operand is present either in register or in memory. After processing result is placed in source-1 register.

(b) Register to register reference CPU: In this organisation, ALU operations are performed only on register data, means both of the operands are always required in register. After processing result in placed in 3rd register.

Q.3 List five distinct features each of the RISC based and the CISC based design of processors.

Solution:

RISC (Reduced Instruction Set Computer)	CISC (Complex Instruction Set Computer)
It requires multiple clock per instruction.	It requires one clock cycle per instruction.
More number of instruction	Less number of instruction.
More addressing modes	Few addressing mode.
It is hardwired.	It is micro programmed.
It is slower.	It is faster.

Q.4 Distinguish between

(i) High level language and low level language
(ii) Macro-Programming and Micro-Programming
(iii) Machine cycle and instruction cycle
(iv) Hardware interrupt and software interrupt
(v) Memory mapped I/O and I/O mapped I/O

Solution:

(i) Machine specific languages are known as low level language **e.g.** machine language and assembly languages are low level language.

While machine independent languages are high level language **e.g.** C, C++, JAVA, PASCAL.

(ii) Image's built in programming languages can be used to automate complex or repetitive task in case of microprogramming. Microcode is a layer of hardware level instruction and writing microcode is called as microprogramming. Macro instruction is a statement typically for an assembler that invokes a macro definition to generate a sequence of instructions. While microinstruction is hardware level instruction used for implementation of machine code.

(iii) Machine cycle is defined as cycle for accessing memory one time.

While instruction cycle is defined as cycle (total T states) required for execution of an instruction. An instruction cycle contains several machine cycles. **e.g.** MVI M, 20 H contains 3 machine cycle → 1 op-code fetch + 1 read + 1 write.

(iv) A hardware interrupt causes the processor to save its state of execution and begin execution of an interrupt handler.

Software interrupts are usually implemented as instructions in the instruction set, which causes a context switch to an interrupt handler similar to hardware interrupt.

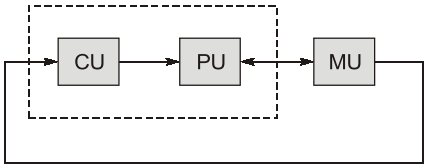
Trigger for hardware interrupt is an electrical signal while for software it is execution of machine language instruction.

(v) In memory mapped I/O address is of 16 bit while in I/O mapped i/o address is of 8 bit. All memory related instructions are used in memory mapped I/O while IN and OUT instructions are only used in case of I/O mapped. Arithmetical or logical operations can be directly performed in case of memory mapped I/O with I/O data while it is not possible in case of I/O mapped.
In case of memory mapped i/o memory is shared between I/Os and system memory. While I/O mapped is independent of memory map.
In case of memory mapped more hardware needed compare to that of i/o mapped I/O.

Q.5 Explain Flynn's classification of computer design?

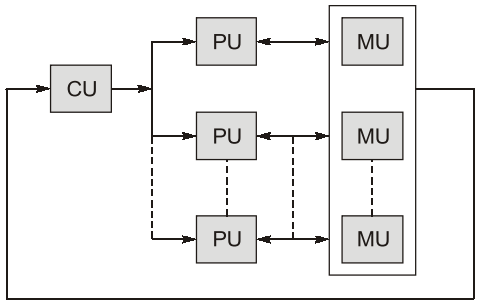
Solution:

(a) **Single Instruction Single Data (SISD) :** No concurrency in this computer.



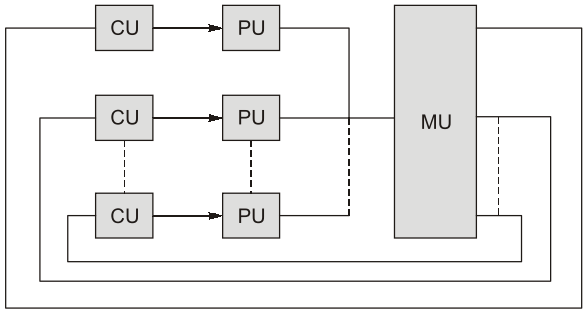
Ex : 8085

(b) **Single Instruction Multiple Data (SIMD) :** Data level concurrency is present

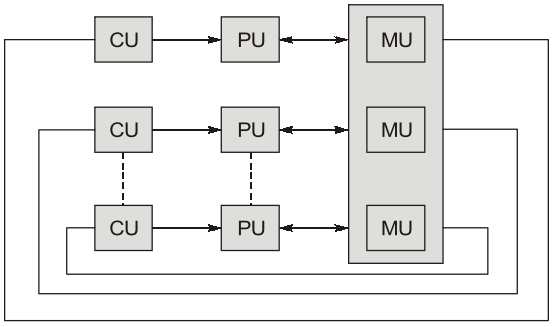


Ex : Staran processor.

(c) **Multiple Instruction Single Data (MISD) :** This architecture contains multiprocessor but only one processor is used at a time.



(d) **Multiple Instruction Multiple data (MIMD) :** This architecture contains instruction level concurrency.



Q.6 Brief about instruction pipeline and evaluate performance gain of the pipeline over non-pipeline system.

Solution:

Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Simultaneous execution of more than one instruction take place in a pipelines processor.

- Pipelined processor has multistage/segments such that output of one stage is connected to input of next stage and each stage performs a specific operation.
- Interface registers are used to hold the intermediate output between two stages. These interface registers are also called latch or buffer.
- All the stages in a pipeline along with the interface registers are controlled by a common clock.

Performance of a pipelined processor:

Consider a 'k' segment pipeline with clock cycle time as 'T_P'. Let there be 'n' tasks to be completed in the pipelined processor.

Now, the first instruction will take 'k' cycles to come out of the pipeline but the other $n-1$ instructions will take only one cycle each. i.e. a total of $(n-1)$ cycles. So, time taken to execute 'n' instructions in a pipelined processor:

$$ET_{\text{pipeline}} = (k + n - 1) \text{ cycles}$$
$$= (k + n - 1)\, T_P$$

For a non-pipelined processor, execution time of 'n' instructions will be

$$ET_{\text{non-pipeline}} = n * k * T_P$$

So, speed up (S) of the pipelined processor over non-pipelined processor, when 'n' tasks are executed on the same processor is

$$S = \frac{ET_{\text{non-pipeline}}}{ET_{\text{pipeline}}}$$

$$S = \frac{(n \times k \times T_P)}{(k + n - 1)T_P} = \frac{n \times k}{(k + n - 1)}$$

When number of tasks 'n' are larger than k,

i.e. $n >> k$

$$S_{\max} = \frac{n \times k}{n} = k$$

$$S_{\max} = k$$

$$\text{Efficiency} = \frac{\text{Given speed up}}{\text{Max. speed up}}$$

$$\eta = \frac{S}{S_{\max}} = \frac{S}{k}$$

$$\eta = \frac{(n \times K)}{(K + n - 1)K} = \frac{n}{K + n - 1}$$